REPORT DOCUMENTATION PAGE

AFRL-SR-AR-TR-02-

0261

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
		01 APR 01-30 APR 02

4. TITLE AND SUBTITLE
GPS SOFTWARE RADIO DIRECT RF SAMPLING RESEARCH

5. FUNDING NUMBERS
F49620-01-1-0482

6. AUTHOR(S)
PROFESSOR ENGE

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
STANFORD UNIVERSITY
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AFOSR/NM
801 N. Randolph Street Room 732
Arlington, VA 22203-1977

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
F49620-01-1-0482

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE, DISTRIBUTION UNLIMITED

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The future satellite positioning navigation systems will provide civil signals an multiple frequencies, similar to that currently available only for military pie. The multiple distinct frequencies will provide many advantages to users of the navigation systems. This report presents the development of a direct RF sampling front end design well suited for multiple frequency satellite navigation receiver design. No frequency down conversion is necessary, rather the particular frequency bands of interest are intentionally aliased using a wide band Maxim 104 analog-to-digital converter (ADC). The resulting samples are passed, via a buffering FPGA design, to the memory space of a host PC far storage as well as eventually processing of the multiple frequency transmission. This paper describes the design of the front-end, validates its concept with collected data. The system designed was demonstratcd at Wright Labs and the developed hardware configuration/software was transferred was their use.

20020903 041

14. SUBJECT TERMS			15. NUMBER OF PAGES 9
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT

GPS Software Radio Direct RF Sampling Research

Final Report

Award Number: F49620-01-1-0482

31-May-2002

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A Direct RF Sampling GPS Receiver

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EXECUTIVE SUMMARY

The future satellite positioning/navigation systems will provide civil signals on multiple frequencies, similar to that currently available only for military use. The multiple distinct frequencies will provide many advantages to users of the navigation systems. This report presents the development of a direct RF sampling front end design well suited for multiple frequency satellite navigation receiver design. No frequency down conversion is necessary, rather the particular frequency bands of interest are intentionally aliased using a wide band Maxim 104 analog-to-digital converter (ADC). The resulting samples are passed, via a buffering FPGA design, to the memory space of a host PC for storage as well as eventually processing of the multiple frequency transmissions. This paper describes the design of the front-end, validates its concept with collected data. The system designed was demonstrated at Wright Labs and the developed hardware configuration/software was transferred for their use.

BACKGROUND

The future of civil satellite navigation is multiple frequency transmissions. The current civil GPS signal consists of a single frequency transmission on 1575.42 MHz, designated L_1. GPS is scheduled to add an additional civil signal at 1227.6 MHz, designated L_2, where currently only a military-specific signal exists. Later modernization efforts will add a third civil frequency signal at 1176.45 MHz, that is designated L_5.

Multiple frequencies will greatly enhance satellite navigation. One of the most commonly referenced limitations with GPS is the vulnerability of the L_1 signal to radio frequency interference – either intentional or unintentional. The received L_1 signal power is extremely weak, specified at -160 dBW. Frequency diversity will greatly improve this potential limitation of the system. In addition, multiple frequencies will provide ionosphere estimation capabilities – removing one of the most significant error sources in the current standalone GPS system. Lastly, the signal structure proposed for the additional GPS frequency on L_5 is designed to have a chipping rate of 10x that currently on the L_1 signal and that being proposed for the L_2 frequency. The higher chipping rate and associated wider bandwidth will also improve performance. Further details on the future GPS signals and the associated advantages are available in the proposed signal designs [1, 2].

The receiver, however, becomes more complicated as it is designed to process multiple frequencies. The primary purpose of any satellite navigation receiver is to determine time of transmission of electromagnetic waves. When multiple frequencies are involved, the front end design becomes much more complex. This is a result of the various mixing stages necessary in a traditional receiver design. In addition, it is critical to have equivalent propagation delays for each frequency band, or be able to calibrate any difference, as to not bias the time estimate.

An elegant approach to the multiple frequency front end design challenge is to use direct radio frequency (RF) sampling of the signal with intentionally aliasing of the information bands. Such an approach is outlined in [3] where direct RF sampling was used to capture satellite navigation signals from the US GPS and Russian GLONASS systems. In this approach no mixing is utilized, rather frequency translation occurs via aliasing of the desired input through the sampling processing. This technique is described in further detail in reference [3] and summarized in the next section.

Although no civil signals on L_2 and L_5 are currently available, it is possible to construct prototype multiple frequency GPS receiver designs to take advantages of the signals which are currently available [4]. As such the design is not practical as a general purpose receiver, but the design process itself will be invaluable for future multiple frequency receiver designs.

An example is the rarely used L_3 transmission. This signal, at 1381.05 MHz, is for nuclear detection capabilities and on very infrequently. However, if a data set can be collected during a period in which L_3 is on and then stored, it too can be post-processed allowing development of the algorithms. Finally, a combination of both examples can be used to capture L_1, L_2 and L_3 usable signals.

The proposed front end design can be easily adjusted to allow for processing of the true GPS civil signal on L_5 the first day it is available. The design experience gained through first developing the $L_1L_2L_5$ receiver will expedite the design of prototype receivers for the actual civil system when it is available.

FRONT END DESIGN AND DIGITAL INTERFACING HARDWARE

Figure 1 shows a block diagram of the hardware equipment used in the system. A GPS antenna is connected to an analog front end. The RF output from the front end is fed directly to an analog-to-digital converter (ADC) without any down conversion stages. The digital output from the ADC is passed to a commercial Field Programmable Gate Array (FPGA). The FPGA is, in turn, interfaced with a CardBus controller for communication with a host PC. The FPGA is configured to buffer samples and transfer that data to the portable PC, via the CardBus interface, using Direct Memory Access (DMA) transfers for data processing. The host PC can then be used for data storage and processing of the collected data.

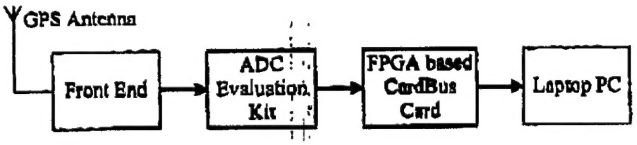

Figure 1. Hardware Configuration

In the following sections the front end, the ADC evaluation kit and FPGA interface design will be described in more detail.

Front End

The traditional front end for a single frequency receiver is depicted in Figure 3. Extending such a design for multiple frequency bands and compensating for all the interfrequency channel biases is by no means a trivial task. In addition, the spurious and harmonics possible can degrade receiver performance and offer the potential for interference issues at intermediate frequency (IF) stages.

The front end proposed for the multiple frequency GPS receiver uses the novel approach of direct RF sampling [3]. A direct RF sampling front end for processing a single frequency band is depicted in Figure 3.

In a direct RF sampling approach, no frequency mixing is done. Rather the signal is sampled direct at the RF carrier frequency. In such a design it is not necessary to sample the signal at twice the carrier frequency, rather frequency translation is accomplished through intentional aliasing of the frequency band(s) of interest. As such, the sampling frequency needs only to be on the order of twice the bandwidth of interest. This direct RF sampling and aliasing process is depicted in the frequency domain in Figure 4.

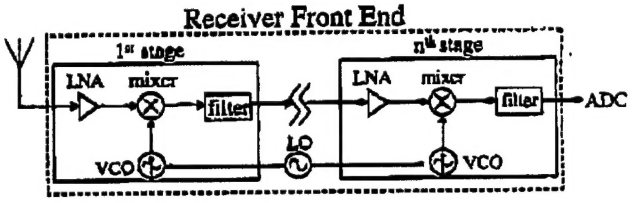

Figure 2. Traditional Front End Design

An advantage of such a design is that is that it is easily extendable to multiple distinct frequency bands – exactly what is required for the future of GPS.

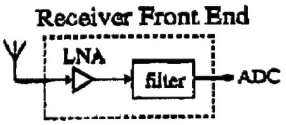

Figure 3. Direct RF Sampling Front End Design

The modification from single to dual frequency is relatively simple – a second bandpass filter is added in parallel with the first as is shown in Figure 5 and the corresponding frequency domain representation is in Figure 6.

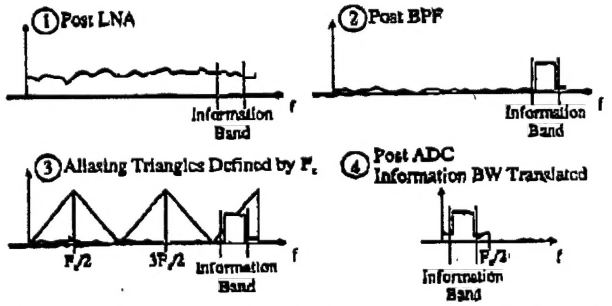

Figure 4. Frequency Domain Representation of Bandpass Sampling

Although the concept is illustrated for only two distinct frequency bands, it can be further extended for additional bands through the incorporation of an additional bandpass filter. In the case of multiband sampling, the minimum sampling frequency is twice the sum of all the individual bandwidths of interest. It is also important to recognize that the resulting aliased IF is a function of the initial

carrier frequency and sampling frequency. These two parameters completely specify the outcome. The nonlinear process of computing the resulting sampling frequency is specified in [3].

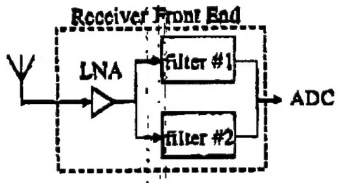

Figure 5. Multiband Direct RF Sampling Design

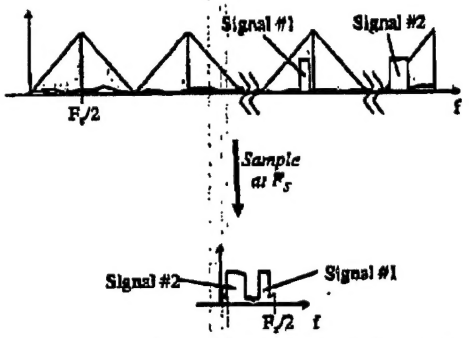

Figure 6. Frequency Domain Representation of Multiband Bandpass Sampling

For this initial work, two distinct front end designs have been implemented. The first is a single L_1 band front end design, as depicted in Figure 3, with a filter bandwidth of 3.2 MHz which can be used to capture the existing Coarse/Acquisition (C/A) code signal. The second design is an implementation of Figure 5 using the same 3.2 MHz L_1 filter with an added 20.0 MHz L_3 filter in parallel. Such an implementation can be used to continually capture data on L_1 and monitor for the presence of a signal on L_3. The filter shapes, taken from a spectrum analyzer, are shown in Figures 7 & 8.

Analog-to-Digital Converter (ADC)

In order to capture the high frequency content in direct RF sampling, an ADC with a wide analog input bandwidth must be utilized. The 8-bit ADC used, a Maxim MAX104 [4], is capable of 1 Gsps conversion rate and has a 2.2 GHz analog input bandwidth. In this application the high conversion rate is not necessary since the RF signal is intentionally aliased down to an intermediate frequency.

The MAX104 ADC is a flash ADC, also known as a parallel ADC. Flash ADCs are suitable for applications requiring relatively high sampling frequencies, but this comes at the expense of high power consumption, relatively low resolution and high cost. However in the case of GPS signals, data is commonly digitized to 1-4 bits which allows the use of a less complex ADC. As such the MAX104 greatly exceeds the requirements for direct RF sampling of GPS and is used as a result of its immediate availability. It is highly probably a significantly less complex design could be used for high volume production, if so desired.

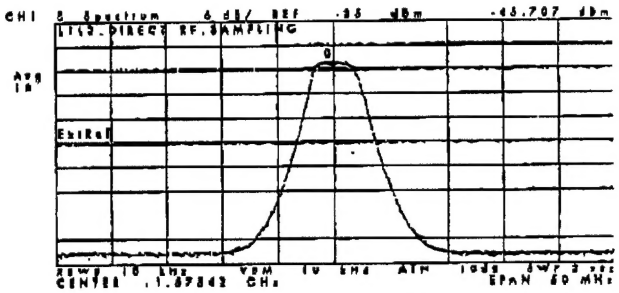

Figure 7. GPS L_1 Bandpass Filter Shape

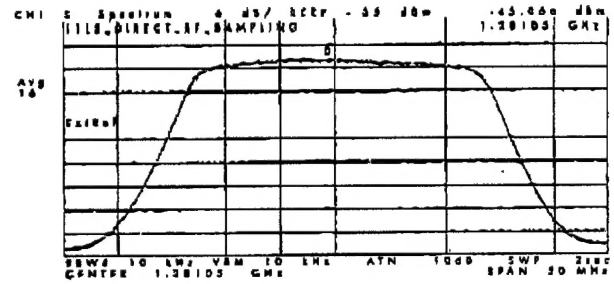

Figure 8. GPS L_3 Bandpass Filter Shape

The digital outputs from the ADC are differential Positive Emitter Coupled Logic (PECL) outputs or Low Voltage PECL (LVPECL). In order to reduce the rate of the digital outputs, two consecutive samples may be presented on two different 8-bit ports, i.e. the ADC chip may be set to perform a 8:16 de-multiplexing.

The MAX104 ADC Evaluation kit set-up in the laboratory with the appropriate connections as is shown in Figure 9.

FPGA-based CardBus Card

One of the most critical elements in the design is the interfacing of the digital samples from the ADC with a storage/processing platform. This will allow to the development of the desired signal processing algorithms, initial in a post processing environment which can then be eventually transitioned to a real time implementation.

In order to interface the ADC with a storage system a commercial CardBus card is used. A block diagram of the card is shown in Figure 10.

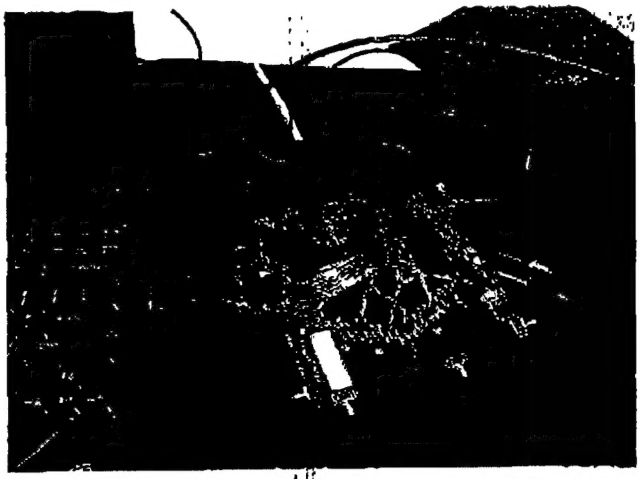

Figure 9. MAX104 ADC Evaluation Board and Associated Interfaces

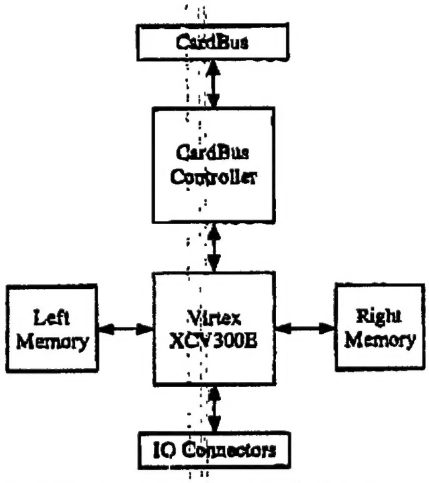

Figure 10. CardBus Card Architecture

Such a configuration is ideal as it allows storage of collected data in the usually large memory buffers on a host computer. In addition, the computer will provide a convenient means in which to process and analyze the collected data.

The key element on the card is the Field Programmable Gate Array (FPGA) as this is the component responsible for providing the bridge between the ADC and host computer.

A generic FPGA consists of an array of programmable logic blocks surrounded by I/O blocks, connected with programmable interconnect as illustrated in Figure 11. Other blocks such as phase locked loops, blocks of SRAM, and dedicated resources for arithmetic operations are common in different FPGA vendor architectures. The FPGA on the CardBus card is SRAM based, which means that its configuration is stored internally in SRAM. Hence an SRAM based FPGA can easily be reconfigured for various applications.

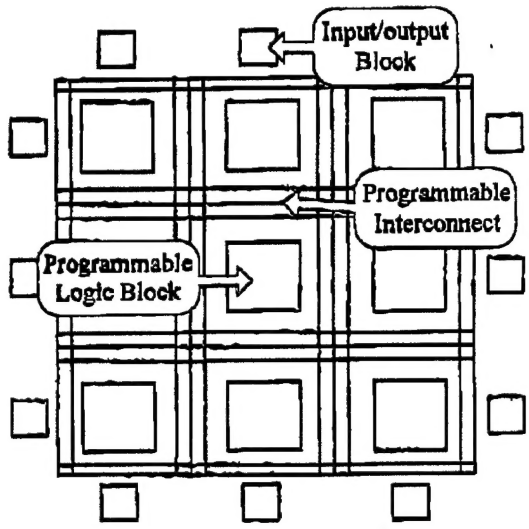

Figure 11. A Generic FPGA Architecture

The FPGA on the card, a Xilinx Virtex XCV300E device [6], is connected to a 32-bit 33 MHz CardBus controller, two 256 kbyte SRAMs and two 13-bit I/O connectors. The card is capable of DMA transfers which allows a theoretical transfer rate of up to 132 MB/s.

The card comes with VHDL libraries to aid in hardware development. Software drivers and an "Application Programming Interface" (API) for the card are available for Microsoft Windows 2000 and Linux.

FPGA Design

The input/output (I/O) ports on FPGA can be configured to support a variety of different single-ended and differential I/O standards. The Virtex-E device is somewhat unique as it is one of the few programmable logic devices which supports the differential LVPECL standard. However the CardBus card only has seven differential I/O pairs available for the user. So only six of the eight possible data bits are and one clock have been implement – more than sufficient for GPS processing. A twisted pair cable was made to directly connect the ADC Evaluation board to the CardBus I/O connectors.

A simplified block diagram of the data path implemented in the FPGA is shown in Figure 12. The 6-bit data is converted to 8-bit two's complement format inside the FPGA and de-multiplexed to form a 32-bit word. The 32-bit words are written to an asynchronous FIFO that synchronizes the data to the memory clock domain.

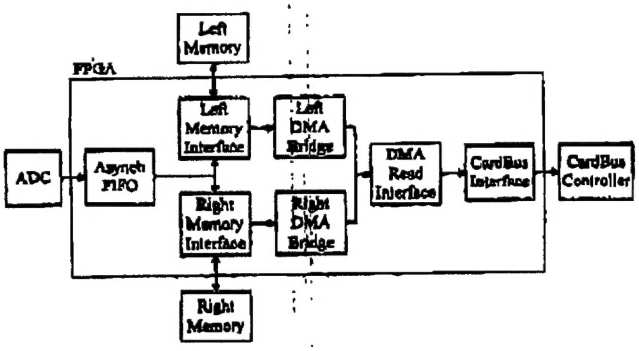

Figure 12. Simplified Block Diagram of Data Path Implemented in the FPGA

The PC, following referred to as the *host*, initiates the data acquisition by writing to a specific register in the FPGA. At initialization the host also sets a programmable decimation rate and how many buffers that should be acquired. One buffer is the size of one SRAM on the CardBus card. The incoming data starts filling the left memory and when the memory is full an interrupt is triggered. This interrupt initiates a transfer of the DMA bridge by starting to fill a FIFO in the DMA Read Interface entity. The host will react to the interrupt and will initiate a DMA transfer via the CardBus. When the host has read the memory it will acknowledge that it is done by writing to a register in the FPGA. Meanwhile the right memory is written to via the asynchronous FIFO. When the right memory is full, another interrupt is triggered when the acknowledge register write from the host is detected. Another DMA transfer from the right memory will then be performed. The complete sequence may be repeated for an arbitrary number of buffers.

If the host does not acknowledge a buffer before the asynchronous FIFO is full, samples will be missed and the interrupt is never triggered. Instead a status register, readable by the host, is set. The host will then time out waiting for the interrupt and then read the status register. At this stage the data acquisition must be reinitiated by the host.

The FPGA design itself does not put the upper bound of the maximum achievable sampling rate for contiguous buffers, instead the upper bound is limited by the practical transfer rate of the CardBus. The FPGA design has been constrained to handle data rates over 120 Mbyte/s.

The data acquisition design was first implemented and tested using a traditional CMOS/TTL level ADC. Once that was functional, the desired LVPECL logic interface required for the MAX104 ADC was implemented.

VALIDATION OF HARDWARE DESIGN

Two distinct front end designs had been implemented to initiate the multiple frequency GPS receiver prototype. The first design consists of only the traditional L_1 RF processing, digitization, and storage of the samples. This allows the various elements in the system design to be tested. The second design adds the ability to capture the L_3 signal along with the L_1 signal. This implementation is configured to determine the presence of L_3 and saved the captured data when it is present. This will allow the capture of L_1L_3 data, when L_3 is available, that can be used to explore receiver design issues that will parallel those when multiple civil signals are available.

L_1 Direct RF Sampling Implementation

The L_1 only implementation is based on the design depicted in Figure 3. There are subtle differences between the figure and the actual implementation. Rather than a single amplifier, the gain is distributed across three different amplifiers and a second L_1 filter is used between the first and second amplifier. The final L_1 bandpass filter, shown in Figure 7, follows the third amplifier and directly precedes the input to the ADC.

With the analog signal conditioning hardware in place and connected to the ADC, the next step was to determine an appropriate sampling frequency. Again, although the sampling is done on the RF signal directly, it is only necessary to sample at twice the bandwidth of the signal and choose the sampling frequency to appropriately alias the signal. The 3 dB bandwidth of the filter is specified at 3.2 MHz, however the bandwidth is wider at higher attenuation levels. In order to adequately alias the complete band, a sampling frequency on the order of 16 MHz is used. This provides an 8 MHz sampled information bandwidth which is more than sufficient for the final filter shape. A ladder diagram was generated to determine an appropriate sampling frequency about 16 MHz. This is shown in Figure 13 and indicates a sampling frequency of 16.2 will translate the 1575.42 MHz L_1 center frequency to the center of the resulting sampled information bandwidth at an IF of 4.02 MHz.

This configuration was used to collect 2^{20} samples or approximately 60ms of data. Since the GPS signal power is below that of the noise floor, it is expected the captured data should appear as noise in the shape of the final bandpass filter. Figure 14 shows the power spectral density of the collected data samples.

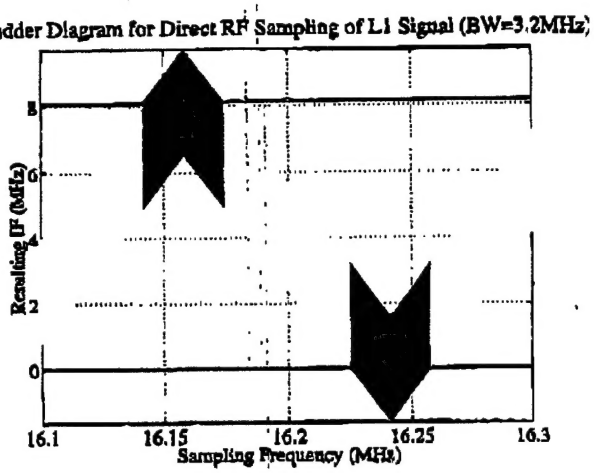

Figure 13. Ladder Diagram for Direct RF Sampling of the GPS L_1 Signal

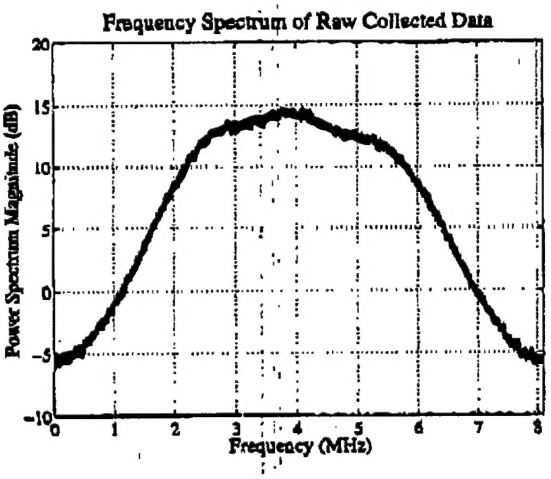

Figure 14. Frequency Domain Representation of Collected Raw Data

The frequency domain depiction of the collected data looks equivalent to that of the filter shown in Figure 7. As such, it is expected that the desired frequency translation of the L_1 band has been accomplished via intentional aliasing. The frequency translation was further confirmed by applying a GPS acquisition algorithm to the collected data and all six satellites in view at the time of the data collection were identified [7]. In addition, once the particular satellite parameters have been identified (PRN number, code phase, and carrier frequency) it is possible to do a correlation of the collected data with a properly aligned PRN code. This operation removes the PRN code modulation leaving the underlying carrier and navigation data bits. If this post-correlation data is viewed in the frequency domain, as is shown in Figure 8, the GPS IF for PRN 24 in the collected data is clearly shown.

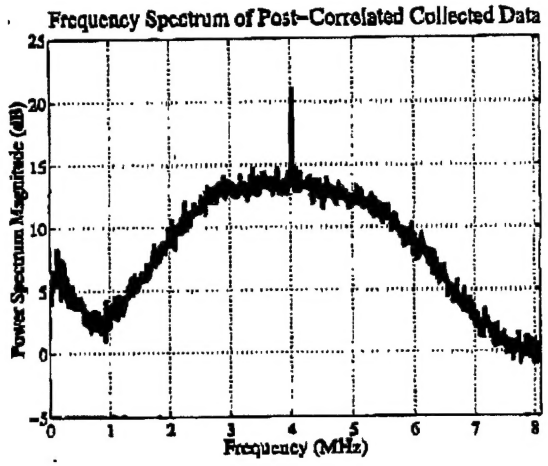

Figure 15. Frequency Domain Representation of Post-Correlated Data

The process has verified the the direct RF sampling and data collection implementation of the single frequency GPS L_1 signal.

L_1L_3 Direct RF Sampling Implementation

With the verification of the single frequency band design, it is possible to extend the concept to multiple frequency bands. Based on the GPS multiple frequency options described in the introduction, the more interesting band is L_3 as there is little documented on that signal. The L_2 signal format is well documented and the best starting point for that signal is through the use of a high gain antenna. As such, the decision was made to implement an L_1L_3 design that would capture the L_1 GPS signal and monitor for the presence of the L_3 transmission.

The L_1L_3 design has been implemented using the structure depicted in Figure 5 with the two filters shown in Figures 7 and 8. The filter bandwidth on L_1 is kept at 3.2 MHz to capture only the C/A spectrum, ignoring the quadrature military-specific P(Y) signal. A 20 MHz bandpass filter, centered at 1381.05 MHz, is the final filter in the L_3 signal path. The wide bandwidth in this path is to allow for the capture of a variety of possible signal structures on the L_3 frequency.

This front end implementation was connected to the antenna and the output, which will be passed to the ADC for sampling, is initially viewed on the spectrum analyzer. This frequency domain representation is shown in Figure 16.

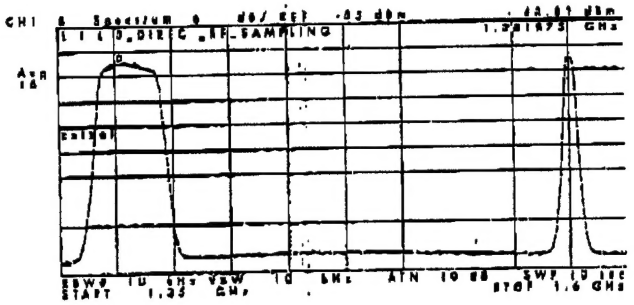

Figure 16. Frequency Domain Representation of the Dual Band Front End Output

The figure shows the frequency span from 1.35 GHz to 1.6 GHz. The two respective bandpass filter shapes are clearly shown. The goal will be to choose a sampling frequency to intentionally alias both these frequency bands yet keep them distinct.

The minimum sampling frequency for this combination is twice the sum of the bandwidths. The filter 3 dB bandwidths are 3.2 MHz and 20 MHz for the L_1 and L_3 filters, respectively. The minimum possible sampling frequency is on the order of 50 MHz. However, in the multiple signal aliasing it is critical to find a sampling frequency in which the resulting aliased bands will not only not cross the information bandwidth boundaries at 0 and $F_s/2$, but also not have overlapping frequency bands. The computation of an acceptable sampling frequency was done according to [3] and it was found that a sampling frequency of approximately 74 MHz would acceptable provide the desired aliasing. The ladder diagram for these two frequency bands, with sampling frequency from 72 MHz to 75 MHz, is shown in Figure 17. The highlighted region shows the range of acceptable sampling frequencies that meet the necessary criteria and the resulting IF of both bands after aliasing.

A sampling frequency from this acceptable band, 73.45 MHz, was used to sample the data from the front end to test the direct aliasing of both frequency bands. The frequency domain representation of this data is shown in Figure 18. The resulting frequency bands are exactly where they are computed to be from the ladder diagram of Figure 17. Further confirming the success of the implementation the GPS acquisition algorithm identified L_1 signals in the data set from all of the satellites visible at the time of data collection. However, no signals could be detected in the L_3 band in the collected data set. It is assumed that at the time of the data collection, there was no L_3 transmission from the satellites. Yet the direct RF sampling and aliasing have been successful and provide the baseline for an L_3 monitor.

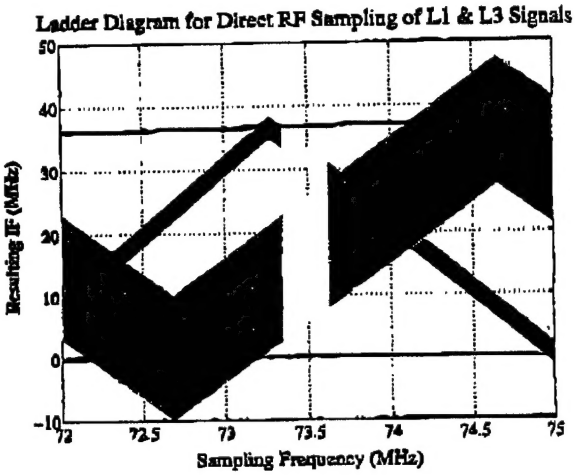

Figure 17. Ladder Diagram for Direct RF Sampling of L_1 and L_3 Bands

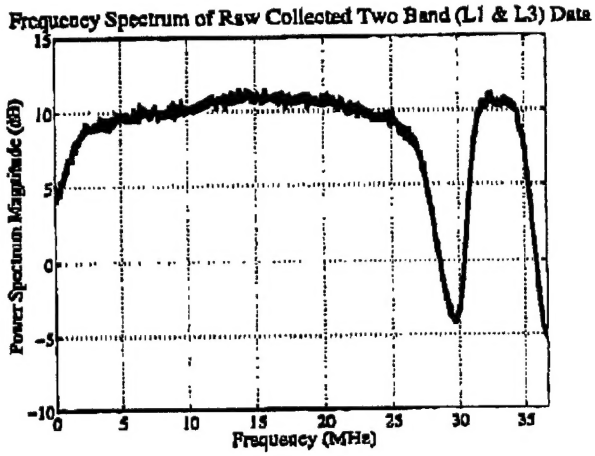

Figure 18. Frequency Domain Representation of the Collected Dual Band Data

CONCLUSIONS & FUTURE WORK

This report has presented the design of a multiple frequency GPS receiver prototype. Multiple frequencies transmissions are the future of GPS-SPS and already exist for military GPS-PPS. The implementation utilizes a novel direct RF sampling approach and an FPGA is used to interface the digital samples with a PC for data storage and analysis. The front end design and data interface have been verified using collected data. A dual frequency implementation collected GPS data on the L_1 and L_3 bands has been designed and was successful used to capture data. Although L_3 was not found to be in the collected data, the platform will serve as an L_3 monitor and is a starting point for multiple frequencies GNSS civil receiver design.

The implementation has shown the feasibility of such an implementation through the acquisition of GPS signals. However, full processing of the GPS transmission must be done in order to validate and compare the direct RF sampling performance to that of a traditional receiver. An additional item of interest is to verify the interference suppression that should be available from such a direct RF sampling receiver. Both of these topics are proposed for future investigation.

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